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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,447	10/26/2004	Hiroshi Takahara	260903US2PCT	4248

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EXAMINER	
CHOWDHURY, AFROZA Y	
ART UNIT	**PAPER NUMBER**
2609	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	03/02/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 03/02/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/511,447	TAKAHARA ET AL.	
	Examiner	Art Unit	
	Afroza Y. Chowdhury	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/26/07, 11/1/05*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following bold line is required:

Regarding claim 8, **an EL display panel, comprising: a display area of I pixel rows (I is an integer larger than 1) and J pixel columns (J is an integer larger than 1).**

Claim Objections

3. Claim 11 is objected to because of the following informalities: the line "**unit transistors which generate the programming current in the source driver circuit are n-channel transistors**" repeated twice. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1–15 are rejected under 35 U.S.C. 102(e) as being unpatentable by Yamano et al. (US 2005/0057580).

As to claim 1, 3, 5, 10, 11, and 15, Yamano et al. discloses a drive method for an EL display panel, the EL display panel comprising: EL elements arranged in a matrix (page 3, [0038], [0053], [0059]); driver transistors which supply current to be passed through the EL elements (page 3, [0067], page 12, [0259]);

first switching elements placed in current paths of the EL elements (page 3, [0067]); a gate driver circuit which turns on and off the first switching elements for control (page [0068]); and a source driver circuit which supplies programming current to the driver transistors (page 12, [0261], fig. 44, page 34, [0498]),

wherein the driver transistors are p-channel transistors (fig.1 page 4, [0071], [0063]), unit transistors which generate the programming current in the source driver circuit are n-channel transistors (fig. 72, page 43, [0610], page 46, [0648], and the gate driver circuit turns off the first switching elements at least two or more times during one frame period or one field period (page 16, [0316] – [0317], page 17, [0322]);

the first gate driver circuit turns off the first switching elements a number of times during one frame period or one field period (page 3, [0061], [0067], page 17,[0322]), the first gate driver circuit is placed or formed on one side of the display panel (fig. 1, page 3, [0067], page 14,[0284]), and the second gate driver circuit is placed or formed on another side of the display panel (fig. 1, page 4, [0069], page 14, [0284]);

a period during which a pixel row is selected and programmed with current is constructed from a first period and second period (page 25 – 26, [0409], [0015]),

a first current is applied during the first period (page 25 – 26, [0409], [0015]), a second current is applied during the second period (page 25 – 26, [0409], [0015]), the first current is larger than the second current (page 2, [0031], [0034]),

the source driver circuit outputs the first current during the first period and outputs the second current during the second period which comes after the first period (fig. 22, 30 - 31, page 25 – 26, [0409], [0415]); and

a receiver (page 72, [0908]-[0909]).

As to claim 2 and 4, Yamano et al. teaches a drive method for an EL display panel wherein the first switching elements are turned off periodically during one frame period or one field period (page 17, [0322], [0324]).

As to claim 6, Yamano et al. teaches an EL display panel according to claim 5, wherein the gate driver circuits are formed in a same process as the driver transistors (page 13, [0267]) and the source driver circuit is made of a semiconductor chip (page 4,

[0073]).

As to claim 7, Yamano et al. discloses an EL display panel, comprising: gate signal lines (fig. 1, page 14, [0280]); source signal lines (fig.1, page 9, [0220]); a source driver circuit which outputs programming current (page 12, [0261], fig. 44, page 34, [0498]); a gate driver circuit (page 17, [0322]);

EL elements arranged in a matrix (page 3, [0038], [0053], [0059]; driver transistors which supply current to be passed through the EL elements (page 3, [0067], page 12, [0259]);

first transistors placed in current paths of the EL elements (page 9, [0225]); second transistors which constitute paths used to transmit programming current to the driver transistors (page 19, [0340]); and

a source driver circuit which supplies programming current to the driver transistors (page 12, [0261], fig. 44, page 34, [0498]), wherein the driver transistors are p-channel transistors (fig.1 page 4, [0071]), unit transistors which generate the programming current in the source driver circuit are n-channel transistors (fig. 72, page 43, [0610], page 46, [0648]),

the source driver circuit outputs programming current to the source signal lines (fig.1, page 12, [0261]), the gate driver circuit is connected to the gate signal lines (fig.1, page 9, [0220]),

gate terminals of the second transistors are connected to the gate signal lines (fig. 1), source terminals of the second transistors are connected to the source signal

lines (fig. 1), drain terminals of the second transistors are connected to drain terminals of the driver transistors (fig. 1), and

the gate driver circuit selects a plurality of gate signal lines and supplies the programming current to the driver transistors of a plurality of pixels (fig. 34, page 30 – 37, [0461], [0468], [0510]).

As to claim 8, Yamano et al. teaches an EL display panel, comprising: a source driver circuit which applies an image signal to source signal lines in the display area (page 2, [0028], fig. 6, page 12, [0261]); a gate driver circuit which applies a turn-on voltage or turn-off voltage to gate signal lines in the display area (fig. 34, page 30 – 37, [0461], [0468], [0510]); and

a dummy pixel row formed outside the display area (fig. 27 and 29, page 25, [0403]), wherein EL elements are arranged in a matrix in the display area (page 3, [0038], [0053], [0059]) and emit light based on the image signal from the source driver circuit, and the dummy pixel row either does not to emit light or emits light not visible to the eye (page 25, [0404]). He also teaches about pixel rows and pixel columns (page 23, [0391]-[0392]).

It is inherent for an EL display comprising I pixel rows (I is an integer larger than 1) and J pixel columns (J is an integer larger than 1).

As to claim 9, Yamano et al. teaches an EL display panel wherein the gate driver circuit selects a plurality of pixel rows at a time and applies the image signal from the

source driver circuit to the plurality of pixel rows (page 25 – 26, [0409], [0015]); and a dummy pixel row is selected when the first pixel row or l-th pixel rows is selected page 25, [0403] – [0406]).

As to claim 12 and 14, Yamano et al. discloses a drive method for an EL display panel, comprising: supplying EL elements with a current which makes the EL elements emit light brighter than a predetermined brightness (fig. 12, page 18, [0333]); making the EL elements emit light for a period equal to 1/N of one frame period or one field period (N is larger than 1) (page 17-18, [0322], [0334]); and shifting the display area of 1/N of the entire screen in sequence to display the entire screen (page 18, [0335]).

As to claim 13, Yamano et al. teaches a drive method for an EL display panel wherein the period equal to 1/N of a frame is divided into a plurality of periods (page 17, [0318]).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Afroza Y. Chowdhury whose telephone number is 571-270-1543. The examiner can normally be reached on 7:30-5:00 EST, 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-272-2600. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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AMARE MENGISTU
SUPERVISORY PATENT EXAMINER